5,219,793 ("Cooper"); rejected claims 4-6, 8-10, 14-16, and 18-20 under 35 U.S.C. § 103(a) as unpatentable over Duane as applied to claims 1-3 and 11-13, and further in view of Cooper; and rejected claims 7, 8, 17, and 18 under 35 U.S.C. § 103(a) as unpatentable over Duane as applied to claims 1-3 and 11-13, and further in view of Chang et al., U.S. Patent No. 6,159,842 ("Chang"), and further in view of Tsai et al., U.S. Patent No. 6,331,480 ("Tsai"). Applicants traverse the objection and rejections for the following reasons.

**Response to Objections**

The Examiner alleged that the antecedent basis for the phrase "conductive layer patterns" is unclear (Office Action, p. 2). In response, Applicants amend claim 1 to change the phrase "conductive layer patterns" to --bit line patterns--. Antecedent basis for this phrase may be found, for example, at claim 1, line 3. In view of this, Applicants request that the Examiner withdraw the objection to claim 1.

Additionally, the Examiner alleged that claims 6 and 16 contain informalities because "it is unclear that how forming a mask pattern covering a top portion of the conductive layer can be formed after an interlayer insulating layer," (Office Action, p. 2) Applicants amend claim 6 to more appropriately define the invention. In view of this, Applicants request that the Examiner withdraw the objection to claim 6. Additionally, Applicants cancel claim 16 without prejudice or disclaimer of the subject matter thereof. Thus, the objection to claim 16 is rendered moot.

**Response to Rejections under 35 U.S.C. § 112, second paragraph**

The Examiner alleged that claims 8 and 18 include improper Markush terminology (Office Action, p. 2). In response, Applicants amend claim 8 as suggested by the Examiner. In view of this, Applicants request that the Examiner withdraw the

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rejection of claim 8 under 35 U.S.C. § 112, second paragraph. Additionally, Applicants cancel claim 18 without prejudice or disclaimer of the subject matter thereof. Thus, the objection to claim 18 is rendered moot.

**Response to Rejections under 35 U.S.C. § 102(e)**

The Examiner rejected claims 1-3 and 11-13 as anticipated by Duane. Applicants cancel claims 11-13 without prejudice or disclaimer of the subject matter thereof. Thus, the rejection of claims 11-13 is rendered moot. In response to the rejection of claims 1-3, Applicants respectfully submit that Duane does not anticipate the claimed invention for the following reasons.

In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102, each and every element of the claim in issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131 (8th Ed., Aug. 2001), quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Finally, "[t]he elements must be arranged as required by the claim." M.P.E.P. § 2131, p. 2100-69.

Claim 1 is directed to a semiconductor device manufacturing method comprising a combination of elements including, *inter alia*, "etching the interlayer insulating layer with an etching mask defining a straight line shape, and forming a straight line shaped contact opening ... forming insulating layers on sidewalls of the bit line patterns."

Duane is directed to a method of fabricating series-connected transistors. Duane discloses forming a dielectric layer 76 and exposing contact regions by etching using a masking layer 80. *See* Duane, Fig. 12 and col. 9, lines 54-67. The Examiner alleged that Duane discloses forming a conductive layer pattern on a substrate; forming an

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inter-level insulating layer; and exposing contact regions by etching the interlayer insulating layer; and forming spacers on sidewalls of the conductive layer patterns (Office Action, pp. 3 and 4). However, Duane does not disclose forming the spacers after forming a contact hole. Duane only discloses forming the spacers with dielectric layer 76 which is left between closely spaced conductors 48 and 50. *See* Duane, col. 9, lines 30-53. Thus, Duane does not teach at least "etching the interlayer insulating layer with an etching mask defining a straight line shape, and forming a straight line shaped contact opening ... forming insulating layers on sidewalls of the bit line patterns." Therefore, Duane fails to anticipate claim 1. For at least this reason, claim 1 is allowable.

Claims 2 and 3 are allowable at least due to their dependence from allowable claim 1.

**Response to Rejections under 35 U.S.C. § 102(b)**

The Examiner rejected claims 11 and 16 as anticipated by Cooper. Applicants cancel claims 11 and 16 without prejudice or disclaimer of the subject matter thereof. Thus, the rejection of claims 11 and 16 is rendered moot.

**Response to Rejections under 35 U.S.C. § 103(a)**

The Examiner rejected claims 4-6, 8-10, 14-16, and 18-20 as unpatentable over Duane as applied to claims 1-3 and 11-13, and further in view of Cooper. Applicants cancel claims 10, 14-16, and 18-20 without prejudice or disclaimer of the subject matter thereof. Thus, the rejection of claims 10, 14-16, and 18-20 is rendered moot. In response to the rejection of claims 4-6, 8, and 9, Applicants respectfully assert that a *prima facie* case of obviousness has not been established for at least the following reasons.

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In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *See* M.P.E.P. § 2143.01, quoting *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. *See* M.P.E.P. § 2143, pp. 2100-122 to 127.

Claims 4-6, 8, and 9 depend from claim 1 and thus incorporate the elements of that claim. As advanced above, Duane fails to teach at least "etching the interlayer insulating layer with an etching mask defining a straight line shape, and forming a straight line shaped contact opening ... forming insulating layers on sidewalls of the bit line patterns." Cooper also fails to teach or suggest this claim element. Cooper merely discloses forming an insulating layer 22 and an etching layer 20 using a photoresist mask 24. *See* Cooper, Fig. 2 and col. 4, lines 38-67. Thus, a *prima facie* case of obviousness has not been established because Duane and Cooper, taken alone or in combination, fail to teach or suggest all the claim elements. For at least this reason, claims 4-6, 8, and 9 are allowable.

The Examiner also rejected claims 7, 8, 17, and 18 as unpatentable over Duane as applied to claims 1-3, and further in view of Chang, and further in view of Tsai. Applicants cancel claims 17 and 18 without prejudice or disclaimer of the subject matter thereof. Thus, the rejection of claims 17 and 18 is rendered moot. In response to the

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rejection of claims 7 and 8, Applicants assert that a *prima facie* case of obviousness has not been established.

Claims 7 and 8 depend from claim 1. As advanced above in the **Response to Rejections under 35 U.S.C. § 102(e)**, Duane fails to teach or suggest at least "etching the interlayer insulating layer with an etching mask defining a straight line shape, and forming a straight line shaped contact opening ... forming insulating layers on sidewalls of the bit line patterns." Likewise, Chang and Tsai fail to teach or suggest at least this claim element. Thus, a *prima facie* case of obviousness has not been established because Duane, Chang, and Tsai, taken alone or in combination, fail to teach or suggest all the claim elements. For at least this reason, claims 7 and 8 are allowable.

In view of the foregoing, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: December 2, 2002

By: _____
Bryan S. Latham
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## Appendix to Amendment of December 2, 2002

**IN THE CLAIMS:**

Please amend claims 1, 6, and 8 as follows:

1. (Amended) [A semiconductor device manufacturing] A method for forming contact openings between bit line patterns, the method comprising the steps of:

a) forming [at least one conductive layer pattern] bit line patterns on a substrate including word line patterns, thereby forming a first resulting structure;

b) forming an interlayer insulating layer on the first resulting structure;

c) etching the interlayer insulating layer with an etching mask defining a straight line shape, and forming a straight line shaped contact opening [exposing contact regions] between [the conductive layer] neighboring bit line patterns; and

d)[ after the step c),] forming [an] insulating [spacer] layers on sidewalls of the [conductive layer] bit line patterns.

6. (Amended) A method of claim 1, [after step b), further comprising a step of:

b1) forming a mask pattern covering a top portion of the conductive layer patterns, wherein the mask pattern is formed of ]wherein top surfaces of the bit line patterns are covered with a layer selected from a group consisting of a silicon nitride layer, a silicon [oxy-nitride] oxynitride layer, and an oxide layer.

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8. (Amended) The method of claim 7, wherein in step c), the interlayer insulating layer is etched by using a gas selected from a group consisting of Ar, $O_2$, $N_2$, $H_2$, $CH_4$, $C_2H_4$, and $C_xF_y$.

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